IN THE CLAIMS:

Claims 1-20 previously canceled without prejudice or disclaimer.

21. (Previously Amended) A semiconductor device, comprising:

a first interconnect metal located on or in a first interlevel dielectric layer;

a second interconnect metal located on or in a second interlevel dielectric layer, the second interlevel dielectric layer located over the first interlevel dielectric layer;

a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over the second dielectric layer; and

a via located through the second and third interlevel dielectric layers and connecting the first and third interconnect metals, the via being void of a landing pad between the second and third interlevel dielectric layers.

Claims 22 and 23 previously canceled without prejudice or disclaimer.

24. (Original) The semiconductor device as recited in Claim 21 wherein the via is a passing metal via with no passing metal feature.

25. (Original) The semiconductor device as recited in Claim 21 further including transistors wherein the first metal feature is located over the transistors and interconnects the transistors to form an operative integrated circuit.

Claim 26 previously canceled without prejudice or disclaimer.

Claims 27 and 28 presently canceled without prejudice or disclaimer.

29. (Previously Added) A semiconductor device, comprising:

a first metal feature located on a semiconductor surface;

a first etch stop layer located on the first metal feature;

a first interlevel dielectric layer located on the first etch stop layer;

a second etch stop layer located on the first interlevel dielectric layer;

a second interlevel dielectric layer located on the second etch stop layer;

an unsegmented via located through the first and second etch stop layers and interlevel dielectric layers, the unsegmented via extending to and contacting the first metal feature and being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer; and

a dual damascene structure adjacent the second metal feature and having a damascene trench portion extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

Claim 26 previously canceled without prejudice or disclaimer.

Claims 27 and 28 presently canceled without prejudice or disclaimer.

29. (Previously Added) A semiconductor device, comprising:

a first metal feature located on a semiconductor surface;

a first etch stop layer located on the first metal feature;

a first interlevel dielectric layer located on the first etch stop layer;

a second etch stop layer located on the first interlevel dielectric layer;

a second interlevel dielectric layer located on the second etch stop layer;

an unsegmented via located through the first and second etch stop layers and interlevel dielectric layers, the unsegmented via extending to and contacting the first metal feature and being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer; and

a dual damascene structure adjacent the second metal feature and having a damascene trench portion extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

230. (Previously Added) The semiconductor device as recited in Claim 29 wherein the unsegmented via is a passing metal via with no passing metal feature.